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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/736,125
Filing Date: December 15, 2003
Appellant(s): PAI ET AL.

Mirut P. Dalal
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on December 12, 2010 appealing from the Office action mailed on April 12, 2010.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

Claims 18-30 are rejected.

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

6,842,219	Lee	1-2005

(9) Grounds of Rejection

The following grounds of rejection are applicable to the appealed claims:

Claims 18-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee (U.S. Patent 6,842,219), hereinafter referred to as Lee.

Referring to claim 18, Lee discloses **a direct memory access controller** (fig. 2, decoding processor 201 with DMA units), said direct memory access controller comprising:

a state logic machine (fig. 4, decoding sequencing control unit DSCU 203a; fig. 2, DSCU 203a; fig. 9, state transition of DSCU 203a; note, each arc of the diagram represents a command or act of a command for transition to another state) for **receiving a single command** (fig. 4, receiving commands from RISC interface 401; col. 10, lines 33-36, data/address/control signals from RISC; fig. 6, coprocessor command for DSCU; col. 4, lines 27-29) to provide **a specified range** (col. 11, lines 15-19, address range of external memory to be accessed; col. 4, lines 27-29,

coprocessor command of access external memory) of **a plurality of sequential data words** (col. 11, lines 62-65, DSCU carries sequential sequence control of MPEG stream; col. 12, lines 38-41, for example, macroblock as data words), wherein the single command expressly states **a starting address** (col. 10, lines 41-46, start address to be used; col. 13, lines 45-52, initial start location of the bus stream) and **an ending address** (col. 10, lines 41-46, end address of the memory to be used; col. 13, lines 45-52, the location of the bit stream up to which decoding is completed) of said specified range; and

a memory controller (fig. 11, buffer controller 1113 of variable length decoder VLD 203ba; fig. 2, VLD 203ba; fig. 12, reversal logic) for fetching **a first portion** (fig. 11, a portion of VLD input buffer 1112; col. 13, lines 27-35, fetch into barrel shift 1104 to lower 32 bit) of the specified selectable range and **a second portion** (fig. 11, a next portion of VLD input buffer 1112; col. 13, lines 27-35, move lower 32 bit to higher 32 and fetch new lower 32 bit) of the specified selectable range after fetching the first portion, wherein the second portion of the range has **a lower address than** (col. 13, lines 27-35, barrel shifter 1104, the new fetch is always shift into lower 32 bit address) the first portion, after the state logic receives the

single command including the starting address and the ending address.

Referring to claim 24, Lee discloses a method for fetching data words, said method comprising:

receiving a single command (fig. 4, receiving commands from RISC interface 401; col. 10, lines 33-36, data/address/control signals from RISC; fig. 6, coprocessor command for DSCU; col. 4, lines 27-29) to provide **a specified range** (col. 11, lines 15-19, address range of external memory to be accessed; col. 4, lines 27-29, coprocessor command of access external memory) of **a plurality of sequential data words** (col. 11, lines 62-65, DSCU carries sequential sequence control of MPEG stream; col. 12, lines 38-41, for example, macroblock as data words) in **a memory** (fig. 2, external memory via 215), wherein the command expressly states a starting at **a beginning address** (col. 10, lines 45-46, start address of the memory) and ending at **an ending address** (col. 10, lines 45-46, end address of the memory) of said range;

fetching a portion (col. 6, lines 58-60, four words), in **a forward address order** (col. 13, lines 33-35, increased address), of the range of **sequential data words** (col. 13, lines 33-35, bit stream), said wherein said portion of the range of sequential data words consists of **a predetermined amount of data words**

(col. 6, lines 58-60, four words) that conclude with and precede the ending address, and wherein the predetermined amount of data words is equivalent to **a capacity of a local buffer** (col. 6, lines 58-60, a one line capacity of a cache memory);

storing (col. 6, lines 58-60, fill the cache memory) the predetermined amount of data words that conclude with and precede the ending address in the local buffer;

fetching, in the forward address order, at least one preceding portion (col. 13, lines 33-35, increased address) of the range of sequential data words, wherein each of the preceding portions of the range of sequential data words consist of the predetermined amount of data words; and

wherein **a one of the preceding portions** (col. 10, lines 49-55, backward decoding; col. 15, lines 49-52, MPEG-4 rewinding and error resilience, the point of error has beginning address) of the range of sequential data words comprises the starting address, truncating those data words that precede the beginning address.

Referring to claim 30, Lee discloses **a system for decoding video data** (fig. 2, MPEG video decoding processor 201 with DMA units), said system comprising:

a memory (fig. 2, external memory via 215) for storing **a packetized elementary stream** (col. 11, lines 62-65, DSCU carries sequential sequence control of MPEG stream; col. 12, lines 38-41, for example, macroblock as data words), said packetized element stream comprising **a plurality of packets** (col. 14, lines 54-55, video packet);

a start code table (col. 10, lines 41-46, DSCU register 403 with DEC memory 203) for **storing starting addresses** (col. 10, lines 41-46, start address) and **ending addresses** (col. 10, lines 41-46, end address) of said plurality of packets;

a video decoder (fig. 2, VDEC 203) for **decoding a particular one of the plurality of packets** (col. 7, lines 12-13, current frame), wherein the video decoder **looks up** (col. 12, lines 46-49, inform DSCU to start decoding) the starting addresses and the ending addresses of the particular one of the plurality of packets and **issues a single command** (fig. 4, receiving commands from RISC interface 401; col. 10, lines 33-36, data/address/control signals from RISC; fig. 6, coprocessor command for DSCU; col. 4, lines 27-29) to fetch the packet, wherein the single command expressly includes **a starting address** (col. 10, lines 41-46, start address to be used; col. 13, lines 45-52, initial start location of the bus stream) and **an ending address** (col. 10, lines 41-46, end address of the memory to be

used; col. 13, lines 45-52, the location of the bit stream up to which decoding is completed) associated with the particular one of the plurality packets; and

a direct memory access controller (fig. 2, decoding processor 201 with DMA units), said direct memory access controller comprising:

a state logic machine (fig. 4, decoding sequencing control unit DSCU 203a; fig. 2, DSCU 203a; fig. 9, state transition of DSCU 203a; note, each arc of the diagram represents a command or act or command for transition to another state) for receiving the single command; and

a memory controller (fig. 11, buffer controller 1113 of variable length decoder VLD 203ba; fig. 2, VLD 203ba; fig. 12, reversal logic) for **fetching a first portion** (fig. 11, a portion of VLD input buffer 1112; col. 13, lines 27-35, fetch into barrel shift 1104 to lower 32 bit) of **a range** (col. 11, lines 15-19, address range of external memory to be accessed; col. 4, lines 27-29, coprocessor command of access external memory), said range comprising **sequential data words** (col. 11, lines 62-65, DSCU carries sequential sequence control of MPEG stream; col. 12, lines 38-41, for example, macroblock as data words) from the starting address to the ending address for the particular one of the plurality of packets, and **a second portion**

(fig. 11, a next portion of VLD input buffer 1112; col. 13, lines 27-35, move lower 32 bit to higher 32 and fetch new lower 32 bit) of the range after fetching the first portion, wherein the second portion of the range has **a lower address than the first portion** (col. 13, lines 27-35, barrel shifter 1104, the new fetch is always shift into lower 32 bit address), after the state logic receives the single command including the starting address and the ending address.

As to claim 19, Lee discloses the direct memory access controller of claim 18, wherein the memory controller fetches the first portion of the range and the second portion of the range in **a forward address order** (col. 13, lines 33-35, increased address).

As to claim 20, Lee discloses the direct memory access controller of claim 18, further comprising: **a local buffer** (col. 6, lines 58-60, the cache memory; and fig. 16, DBC MEM) for storing the first and second portions in **a forward address order** (col. 13, lines 33-35, increased address), said local buffer comprising **a plurality of data words** (fig. 16, DBC MEM, four words).

As to claim 21, Lee discloses the direct memory access controller of claim 20, wherein the plurality of data words of the local buffer are **narrower in width** (fig. 16, DBC MEM with 16 bytes vs. input stream in words) than the sequential data words.

As to claim 22, Lee discloses the direct memory access controller of claim 20, further comprising: **a port** (fig. 12, PMU IN) for transmitting the contents of the plurality of data words of the local buffer in **a reverse address order** (fig. 12, reversal logic).

As to claim 23, Lee discloses the direct memory access controller of claim 22, further comprising: **at least one multiplexer** (fig. 12, multiplexers inside 1203) for reversing the bit positions of contents of **at least one of the data words** (fig. 12, B DO[31:0]) of the local buffer.

As to claim 25, Lee discloses the method of claim 24, further comprising: **loading** (fig. 12, load into CLUST DEC 1202) the portion and the at least one preceding portions of the sequential data words into the local buffer.

As to claim 26, Lee discloses the method of claim 25, further comprising: **reversing** (fig. 12, reversal logic) the portion and the at least one preceding portions of the range of sequential data words.

As to claim 27, Lee discloses the method of claim 26, further comprising: **reversing** (col. 10, lines 49-55, backward decoding; col. 15, lines 49-52, MPEG-4 rewinding and error resilience, the point of error has beginning address) the truncated one of the preceding portions of the range of sequential data words that comprises the beginning address.

As to claim 28, Lee discloses the direct memory access controller of claim 18, wherein the first portion and the second portion are **adjacent to each other** (fig. 14, bit stream forms the first/second portions, stream has adjacent bits).

As to claim 29, Lee discloses the direct memory access controller of claim 18, wherein the specified selectable range of the plurality of sequential data words is **less than** (col. 11, lines 15-19, address range of external memory to be accessed is less than the external memory range) **a memory** (fig. 2, external memory via 215) storing the plurality of sequential data words.

(10) Response to Argument

As initial matter, examiner provides following definitions to assist claim interpretation.

DEFINITION OF "STATE LOGIC MACHINE"

Examiner did a quick Google search where the search result indicates no single identical term as "**state logic machine**";[1] thus the claim is interpreted as non-conventional and based on their broadest reasonable interpretation consistent with all corresponding structure or materials described in the specification and their equivalents including the manner in which the claimed functions are performed.

DEFINITION OF "A SINGLE COMMAND"

"*command n. An instruction to a computer program that, when issued by the user, causes an action to be carried out. Commands are usually either typed at the keyboard or chosen from a menu*" (Microsoft Computer Dictionary, 5th edition).

[1] Google search result, retrieved January 28, 2011.

"*command* n. *Computer Science: A signal that initiates an operation defined by an instruction*" (American Heritage College Dictionary, 4th edition).

Appellant states that Lee does not disclose "a state machine for receive a command" as perceiving that Lee's DSCU (Decoding Sequencing Control Unit) 203a does not receive a command. Appellant asserts that even though the DSCU 203a embodied co-processor interface 402 receives data/address/control signals, the data/address/controls are not command as only opcode is considered as a command (pages 7-8).

Examiner disagrees with appellant as appellant erroneously defined command. Firstly, Lee expressively states **command 501** format used for reading or writing the register of each block included in VDEC 203.[2] Secondly, appellant misleads the argument; for example, on the definitions of command must be opcode.[3] Furthermore, appellant's specification has never mentioned the term opcode equivalent to command.

As to the meaning of opcode, ordinary skilled artisan understands that the plain meaning of opcode is only a portion of an instruction. An instruction may contain both opcode and

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[2] Lee, Col. 10, lines 59-61.
[3] Appeal Brief, page 8, paragraph 2.

operand.[4] Thus, opcode is not a command or an instruction, and opcode has nothing to do with the claimed "a single command".

As appellant expressively admitted that Lee's coprocessor interface 402 receives data/address/control signals at DSCU 203,[5] appellant's specification appears to concord with Lee's signals and DSCU 203. In particular, in specification, paragraph 0034, appellant expressively states "**the command can be accompanied by a control signal indicating that the data words in the address range are to be provided to the MPEG video decoder 445 in the reverse order**".

Appellant followed with assertion that even the coprocessor interface 402 does indeed to receive command from RISC interface 401, the rest of DSCU 203a internal elements does not receive the same command other than a processed signal from the

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[4] Wikipedia, OPCODE, retrieved on January 26, 2011, "In computer technology, an **opcode** (**op**eration **code**) is the portion of a machine language instruction that specifies the operation to be performed. Their specification and format are laid out in the instruction set architecture of the processor in question (which may be a general CPU or a more specialized processing unit). Apart from the opcode itself, an instruction normally also has one or more specifiers for operands (i.e. data) on which the operation should act, although some operations may have *implicit* operands, or none at all. There are instruction sets with nearly uniform fields for opcode and operand specifiers, as well as others (the x86 architecture for instance) with a more complicated, varied length structure."

[5] Appeal Brief, page 8, paragraph 2.

coprocessor interface 402 after the coprocessor interface 402 receiving the command (page 8).

Examiner respectfully points out that appellant unreasonably argues features neither required by the claims nor specified in the specification. In particular, nowhere in claim language requires the same command must be presented at both the receiving and the internally throughout the claimed state logic machine, nor does the specification support appellant's argument that the state logic machine made no alternation of the command internally to other units. At most, the present claim merely requires "a state logic machine for receiving a single command ..."

Appellant further argues that the state transition of DSCU 203a does not show command such that the arcs are conditions rather than commands (pages 8-9).

Lee uses the terminology "condition" 502/602 with command 501/601.[6] As appellant expressively indicates that Lee's arcs are conditions,[7] examiner considers appellant agreeing Lee's arc represents command. Although, Lee never mentions that the state transitions or the arcs are "conditions".

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[6] Lee, figures 5 and 6.
[7] Appeal Brief, page 8, paragraph 5.

As a background of this pertinent art, it is noted that a state transition diagram such as Lee's figure 9 is only meant to mathematically describe an abstract model of a system. A state transition diagram is not for physically illustrating the structure; however, a skilled artisan would know to view the state transition diagram as what it teaches.

Appellant also does not appear explained the "condition" contrary with dictionary definition of "*A signal that initiates an operation defined by an instruction*" as the condition needs at least a signal (input) in the processor based decoding system (state logic machine) in Lee. For the sake of argument, even the arc is a condition, the condition is at least an act of a command; thus command has inherency. Examiner found no reason that a condition cannot be realized or interpreted as a command for triggering transition of a State Transition Diagram in a processer based system.

As Lee discloses a MPEG decoding system using processor, the system would change its operating states such as starting decoding state 901, standby state 909, done state 908, etc. with a provided command, thus the input(s) to each state in the state transition diagram would be command(s). Examiner submits that Lee's processor based systems only changes states as instructed by commands. At the same time, appellant has not provided

evidence that Lee's processor based MPEG decoding system would operate without commands; other than provided irrelevant example of flip-flop would change state based on "conditions".

Lee's state transition diagram does not model simple flip-flop. Appellant's over simplified flip-flop analogy does not equivalent to "a state logic machine" as defined by application, nor does the analogy equivalent to Lee's State Transition Diagram of DSCU 203a. As how close Lee must be to be considered as anticipating the claimed invention, it is noted that appellant also indicates the claimed embodiment may be varying levels integrated, and not limited to the particular embodiment(s) disclosed in paragraphs 0042-0043.

Appellant argues that Lee does not teach "a single command to provide a specified range of a plurality of sequential data words" while perceiving Lee's figures 5 and 6 are not co-processor interface commands (page 9).

Examiner respectfully disagrees with appellant, because appellant erroneously understands the meaning of coprocessor and coprocessor commands in Lee. Apparently appellant does not consider VDEC as coprocessor.

Lee discloses a RISC processor 207 with VDEC 203 as one of its coprocessor. The RISC processor 207 communicates with

coprocessor VDEC 203 via coprocessor bus 202 as disclosed in figure 2. Lee mentions "coprocessor command" in figures 5 and 6 as recognized by appellant; however, Lee mentions nothing on "coprocessor interface command". Examiner is unclear where appellant realizes the never disclosed terminology "coprocessor interface command" from Lee.

Lee states that the figures 5 and 6 are command sets used at the coprocessor interface 402 [by coprocessors from RISC processor 207],[8] and the commands are used for reading or writing the registers of each block included in VDEC 203 where VDEC 203 includes DSCU 20a.[9]

Appellant further argues that Lee's command 601 does not disclose "expressively states a starting address and an ending address of said specified range".

Examiner respectfully disagrees with applicant. Lee's commands identify the necessary blocks to be accessed from memory. Each identified memory block will have its corresponding starting and ending addresses. The implicit or explicit specified starting and ending addresses is required to correctly retrieve data from memory.

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[8] Lee col. 10, lines 33-36.
[9] Lee, col. 10, lines 57-61.

It is also noted that the original specification discloses no example of a command expressly stating starting and ending address of a range. The claim clause "the single command expressly states a starting address and an ending address of said specified range" are also results of Claim amendment filed on December 11, 2009. Thus, in view of prosecution history, examiner considers appellant agrees the claim amendment made on December 11, 2009 would be necessary to overcome the cited Lee. However, examiner found very broad and weak support from appellant's specification on the newly amended limitations. As the specification gives no specific requirement of the meaning of the claimed clause, examiner's broadest reasonable interpretation applied. Therefore, the level of "expressly state" is the level of explicitly in the specification which is found to be none.

At most, appellant discloses a starting address and ending address of a video packet.[10] However, the starting and ending addresses are corresponding to a look up table, namely start code table 507, not the claimed single command. Meanwhile, examiner relies on Lee's starting address and ending address of MPEG packet stream which is consistent with appellant's specification as well.

Appellant argues that Lee dose not disclose "a second portion of the specified selectable range after fetching the first portion, wherein the second portion of the range has a lower address than the first portion" (page 13).

Examiner respectfully disagrees with appellant. Lee indicates that the barrel shifter 1104 moves the lower 32 bit date into the upper 32 location, and at the same time fills the lower 32 bit with new data from bit stream to the input buffer 1112.[11] Thus, the new incoming bit stream data are always at lower address range.

Appellant argues that Lee does not teach "a first and second portion" of buffer with sole reason that Lee discloses a single VLD buffer (pages 14-15).

Examiner respectfully disagrees with appellant, as appellant discloses a single buffer as well.

At last, examiner perceives appellant's intention on seeking patent after a particular MPEG bit stream reversing approach with a reverse signal to a multiplexer (mux) 555 as

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[10] Application, specification, paragraph, 0029, lines 7-9.
[11] Lee, col. 13, lines 27-35.

shown in figure 5, abstract and invention title. However, Lee discloses the same reversing approach with reversal section 1305 and reversible variable length decoder RVLD 203bb as in figures 2 and 12. Moreover, appellant does not expressively claim such a structure as shown in figure 5, nor does appellant argues the claims[12] for such a reverse signal operation. Therein, examiner considers that appellant concedes on Lee disclosing the claimed bit reversal operations. The argued claim limitations are generically broad to any applications as well as unspecific to the reversal bit order in appellant's invention endeavor.

[12] Appellant does not argue all claims. For example, claims 22-23, 26-28 which deal with bit reversal.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/CHENG-YUAN TSENG/

Primary Patent Examiner

Art Unit 2184

Conferees:

/Henry W.H. Tsai/

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